

Complementary Silicon Plastic Power Transistors for Isolated Package Applications

MJF31C (NPN), MJF32C (PNP)

Designed for use in general purpose amplifier and switching applications.

Features

- Collector–Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.2 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- Collector–Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 100 \text{ Vdc (Min)}$
- High Current Gain – Bandwidth Product
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mA}$
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation
- Pb–Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current Unclamped Inductive Load Energy (Note 1) – Continuous – Peak	I_C	3.0 5.0	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	28 0.22	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0 0.016	W W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (Note 1)	E	32	mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

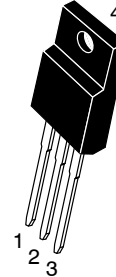
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JC}$	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	4.46	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $I_C = 1.8 \text{ A}$, $L = 20 \text{ mH}$, P.R.F. = 10 Hz, $V_{CC} = 10 \text{ V}$, $R_{BE} = 100 \Omega$.

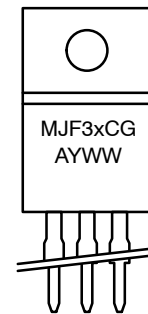
*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

3.0 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 100 VOLTS, 28 WATTS



TO–220 FULLPAK
CASE 221D
STYLE 2

MARKING DIAGRAM



x = 1 or 2
G = Pb–Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJF31C	TO–220 FULLPAK	50 Units/Rail
MJF31CG	TO–220 FULLPAK (Pb–Free)	50 Units/Rail
MJF32C	TO–220 FULLPAK	50 Units/Rail
MJF32CG	TO–220 FULLPAK (Pb–Free)	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (Note 2) ($I_C = 30\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	100	-	Vdc
Collector Cutoff Current ($I_C = 3.0\text{ A}$, $V_{CE} = 4.0\text{ V}$)	I_{CEO}	-	0.3	mA
Collector Cutoff Current	I_{CES}	-	200	μA
Emitter Cutoff Current ($V_{BE} = 5.0\text{ V}$, $I_C = 0$)	I_{EBO}	-	1.0	mA
ON CHARACTERISTICS (Note 2)				
DC Current Gain ($I_C = 1.0\text{ A}$, $V_{CE} = 4.0\text{ V}$) ($I_C = 3.0\text{ A}$, $V_{CE} = 4.0\text{ V}$)	h_{FE}	25 10	- 50	-
Collector-Emitter Saturation Voltage ($I_C = 3.0\text{ A}$, $I_B = 375\text{ mA}$)	$V_{CE(sat)}$	-	1.2	Vdc
Base-Emitter On Voltage ($I_C = 3.0\text{ A}$, $V_{CE} = 4.0\text{ V}$)	$V_{BE(on)}$	-	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain - Bandwidth Product ($I_C = 500\text{ mA}$, $V_{CE} = 10\text{ V}$, $f_{test} = 1.0\text{ MHz}$)	f_T	3.0	-	MHz
Small-Signal Current Gain ($I_C = 0.5\text{ A}$, $V_{CE} = 10\text{ V}$, $f = 1.0\text{ kHz}$)	h_{fe}	20	-	-

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

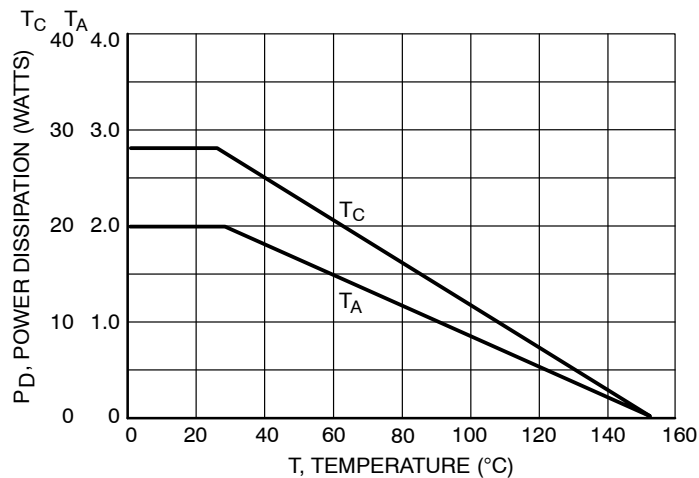
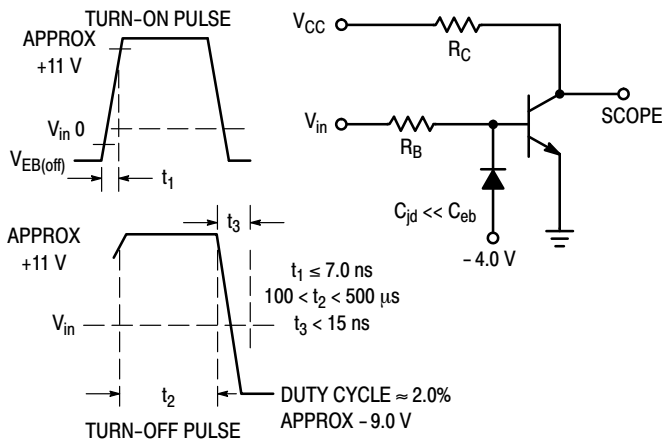


Figure 1. Power Derating

MJF31C (NPN), MJF32C (PNP)



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
Figure 2. Switching Time Equivalent Circuit

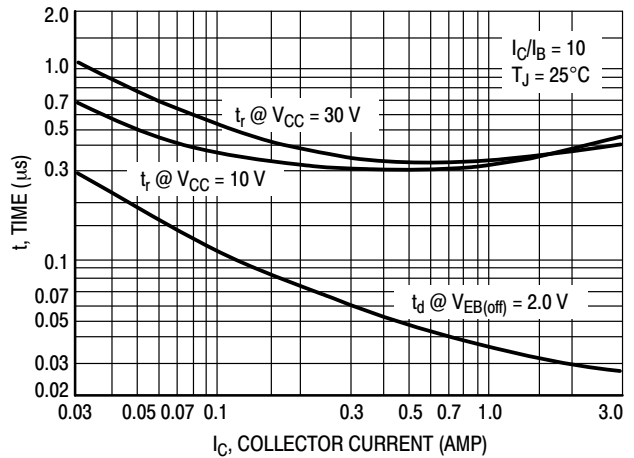


Figure 3. Turn-On Time

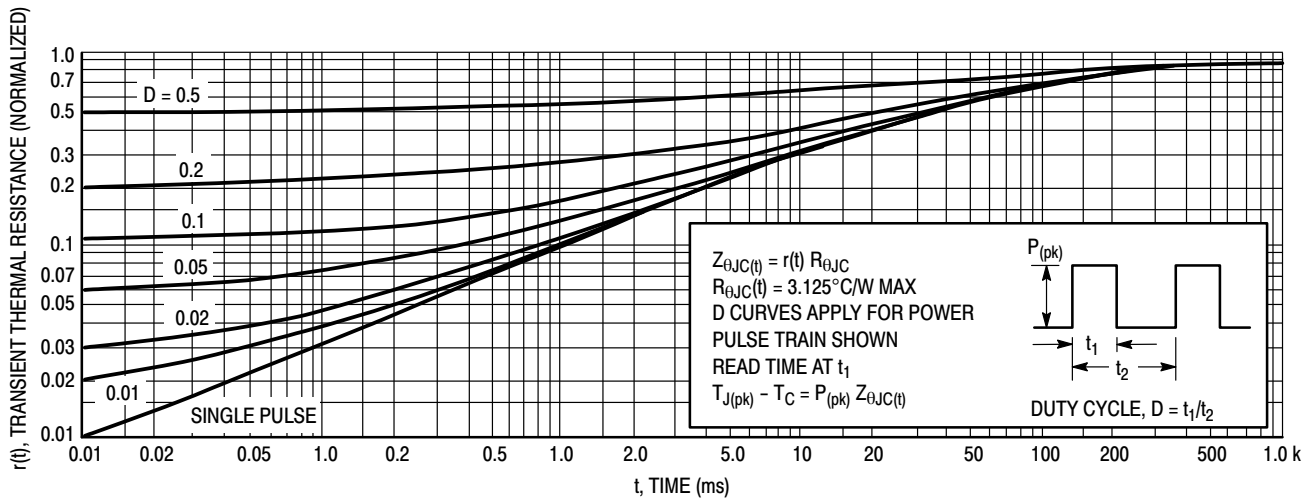


Figure 4. Thermal Response

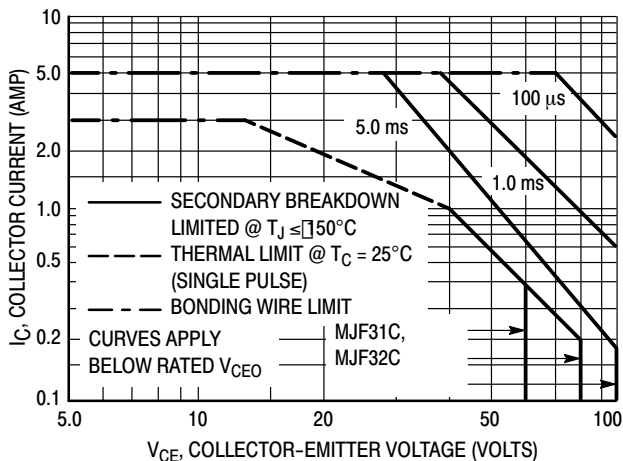


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJF31C (NPN), MJF32C (PNP)

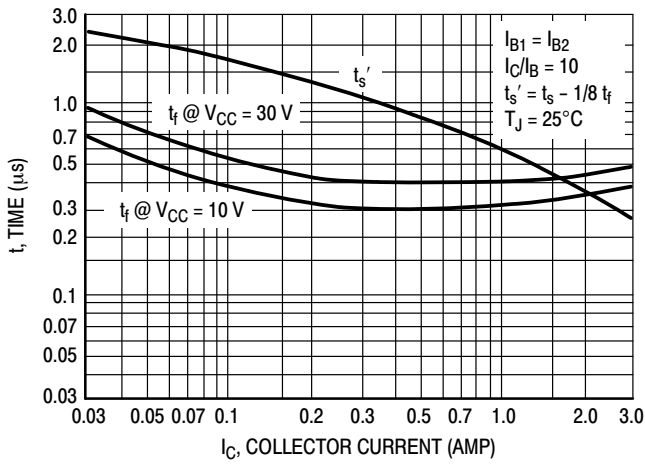


Figure 6. Turn-Off Time

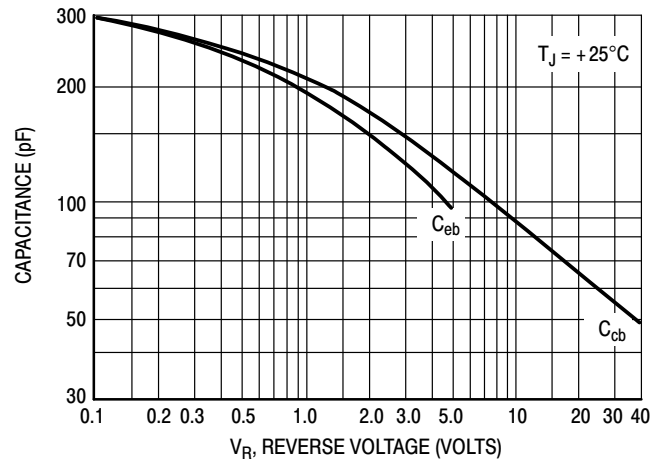


Figure 7. Capacitance

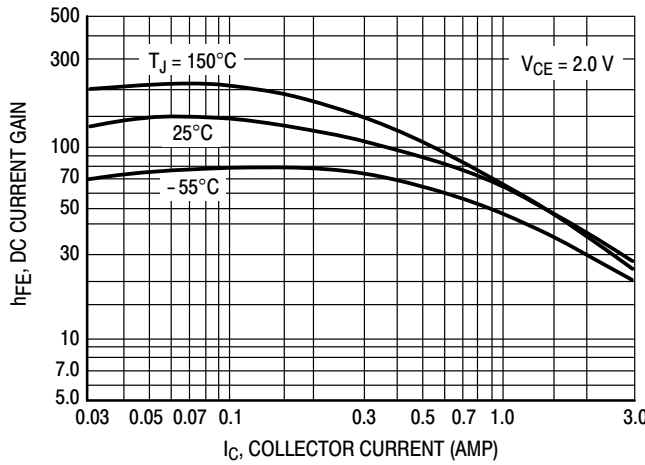


Figure 8. DC Current Gain

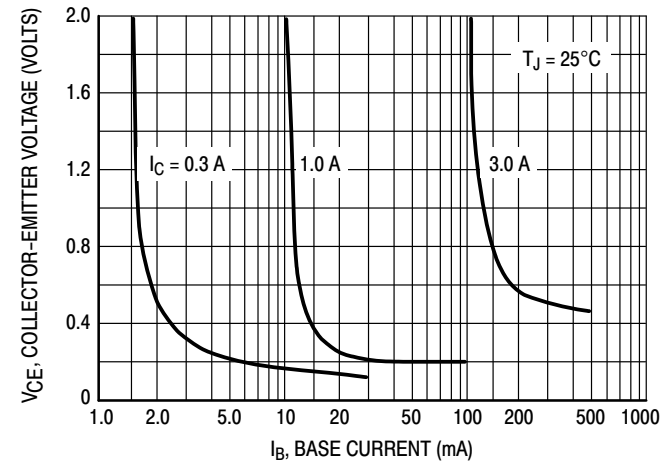


Figure 9. Collector Saturation Region

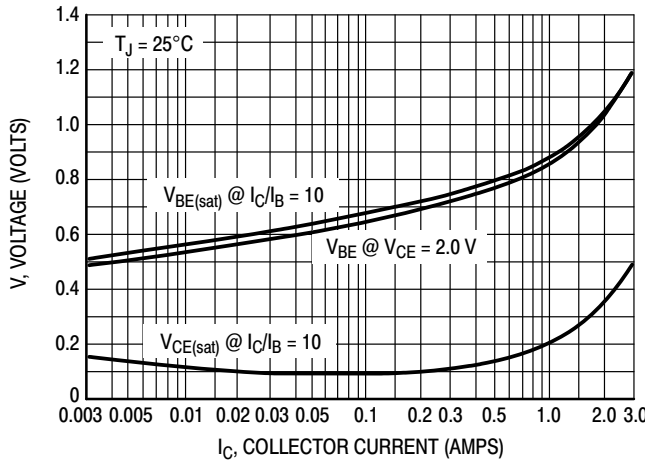


Figure 10. "On" Voltages

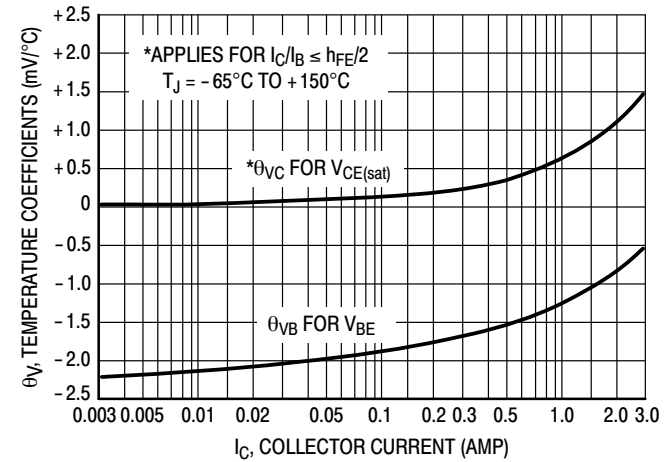


Figure 11. Temperature Coefficients

MJF31C (NPN), MJF32C (PNP)

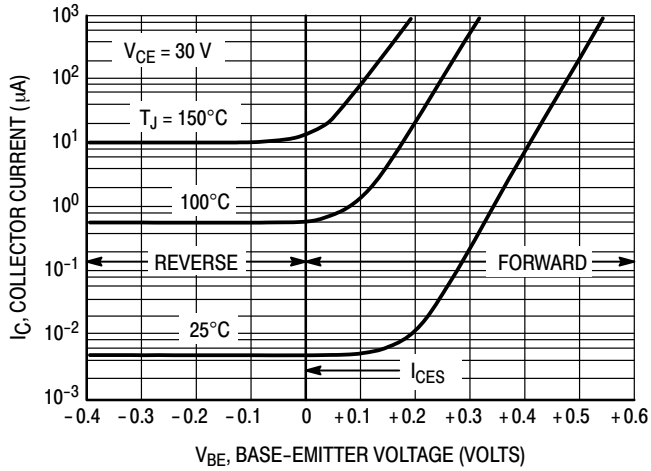


Figure 12. Collector Cut-Off Region

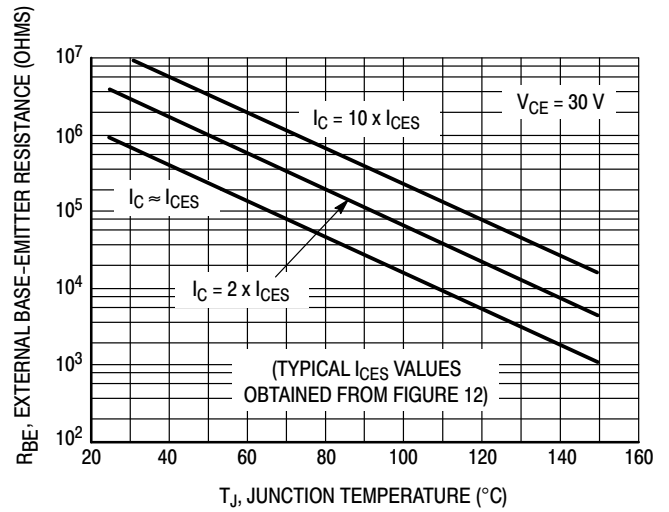
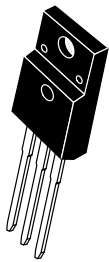


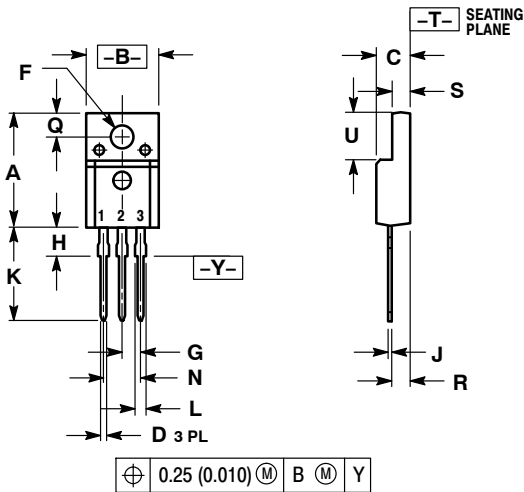
Figure 13. Effects of Base-Emitter Resistance



SCALE 1:1

TO-220 FULLPAK
CASE 221D-03
ISSUE K

DATE 27 FEB 2009



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH
 3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

⊕ 0.25 (0.010) Ⓜ B Ⓜ Y

- | | | |
|--|---|--|
| STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE | STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE |
| STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE | STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE | STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE |

MARKING
DIAGRAMS



Bipolar



Rectifier

- | | |
|-------------------------------|---------------------------|
| xxxxxx = Specific Device Code | A = Assembly Location |
| G = Pb-Free Package | Y = Year |
| A = Assembly Location | WW = Work Week |
| Y = Year | xxxxxx = Device Code |
| WW = Work Week | G = Pb-Free Package |
| | AKA = Polarity Designator |

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